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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,755	09/11/2006	Bartlomiej Jan Pawlak	NL040276	9871

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EXAMINER	
CAMPBELL, SHAUN M	

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
09/23/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/598,755	PAWLAK, BARTLOMIEJ JAN	
	Examiner	Art Unit	
	SHAUN CAMPBELL	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment A, received 7/15/2008, has been entered into the record.

2. Claims 1-19 are pending, claims 1-11 are amended and claims 12-19 are new.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the legal phraseology often used in patent claims, such as "means" and "said," should be avoided. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 7, 9-15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over An et al. (US Patent No. 6,245,618 B1) in view of Mehrad et al. (US Pub. No. 2003/0207527 A1).

7. As to claims 1 and 7, An discloses a method of manufacturing a semiconductor device comprising a field effect transistor (col. 1, lines 6-11), in which method a semiconductor body of silicon (semiconductor substrate 50, figs 5-17) is provided at a surface thereof with a source region and a drain region of a first conductivity type (n-type source/drain regions 80, figs 8-17; col. 3, lines 28-29), which regions are both provided with extensions (source/drain extensions 60, figs 6-17 and col. 3, lines 22-24), and with a channel region of a second conductivity type (fig. 13, p-type implant D), opposite to the first conductivity type (n-type implants A+B), between the source region and the drain region (the space between source/drain extensions 60 as shown in figs 12-17, which is a p-type semiconductor substrate 50; col. 3, lines 20-22), and with a gate region (gate electrode 170, fig 17) separated from the surface of the semiconductor body by a gate dielectric (gate dielectric layer 150, fig 17) and situated above the channel region (fig 17), and wherein a pn-junction between the extensions and a neighboring part of the channel region is formed by two implantations (fig 6 and 8 together formed the first implantation in the source/drain extensions 60 and regions 80 and fig 13 the retrograde impurity region 130) of dopants of opposite conductivity type (the retrograde impurity region 130 in the second implantation has a p-type conductivity

opposite to the n-type source/drain extensions 60 and regions 80 in the first implantation; col. 3, lines 22-29 and 60-61), and characterized in that said two implantations of dopants of opposite conductivity type are performed before the gate region is formed (everything is formed before the gate electrode 170 is formed in fig 17) and at an angle with the surface of the semiconductor body which is substantially equal to 90 degrees (all the implantations are 90 degrees as shown in figs 6, 8, 12 and 13) [claim 1].

An does not disclose wherein an amorphizing implantation is performed before said two implantations [claim 1]; or

that the two implantations are annealed at a temperature between 500 and 700 degrees Celsius [claim 7].

However, An does disclose an amorphizing implantation is performed after said two implantations (fig 12, buried amorphous region 120, col. 3, lines 39-50).

Mehrad discloses pre-amorphization implantation that is used to aid in diode junction formation ([0022] lines 8-10)[claim 1]; and

annealing implantations at a temperature between 500 and 700 degrees Celsius ([0023] lines 1-7)[claim 7].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the amorphization implantation as disclosed in both An and in Mehrad before forming the extensions in the junction region and before the dopant implant into the channel region as evidenced by Mehrad because it would aid in the junction formation.

8. As to claim 12, An discloses a method of manufacturing a semiconductor device (col. 1, lines 6-11) comprising:

providing a semiconductor body having a surface (semiconductor substrate 50, figs 5-17);

forming source and drain regions of a first conductivity type at the surface of the semiconductor body (n-type source/drain regions 80, figs 8-17; col. 3, lines 28-29);

performing an amorphizing implantation in a region of the semiconductor body where a pn-junction is to be formed (fig 12, buried amorphous region 120 by ion implantation);

performing a first implantation of dopants of the first conductivity type, in at least part of the region where the pn-junction is to be formed, to form source and drain extensions of the first conductivity type (n-type ion implants A+B, fig 6 and 8 together formed the first implantation in the source/drain extensions 60 and regions 80);

performing a second implantation of dopants of a second conductivity type opposite the first conductivity type, in part of the region where the pn-junction is to be formed, to form a channel region of the second conductivity type, the channel region extending between the source and drain extension, thereby forming the pn junction (p-type ion implant D, figure 13, retrograde impurity region 130, col. 4, lines 8-13);

forming a gate dielectric (fig 15, gate dielectric layer 150) on the surface of the semiconductor body above the channel region; and

forming a gate region on the gate dielectric (fig 17, gate 170),

wherein the amorphizing implantation (fig 12, buried amorphous region 120) and the first and second implantations are performed before the gate region is formed (everything is formed before the gate electrode 170 is formed in fig 17) and at an angle with the surface of the semiconductor body that is substantially equal to 90 degrees (all the implantations are 90 degrees as shown in figs 6, 8, 12 and 13) [claim 12].

An does not disclose wherein the amorphizing implantation is performed before the first and second implantations [claim 12]; or

characterized in that the two implantations are annealed at a temperature between 500 and 700 degrees Celsius [claim 18].

However, An does disclose an amorphizing implantation is performed after said two implantations (fig 12, buried amorphous region 120, col. 3, lines 39-50).

Mehrad discloses pre-amorphization implantation that is used to aid in diode junction formation ([0022] lines 8-10)[claim 12]; and

annealing implantations at a temperature between 500 and 700 degrees Celsius ([0023] lines 1-7)[claim 18].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the amorphization implantation as disclosed in both An and in Mehrad before forming the extensions in the junction region and before the dopant implant into the channel region as evidenced by Mehrad because it would aid in the junction formation.

9. As to claims 2-4, 9-11 and 13-15, An also discloses:

characterized in that a first implantation (Fig. 6 and 8 together formed the first implantation in the source/drain extensions 60 and regions 80) of the two opposite conductivity type implantations (the retrograde impurity region 130 formed in the second implantation has p-type conductivity opposite to the n-type source/drain extensions 60 and regions 80 formed in the first implantation; col. 3, lines 28-29, 60-61) is carried out using a first mask (temporary gate electrode 54, Figs. 6 and 8) covering a first region of the semiconductor body (covers the region below the temporary gate electrode 54 as shown in Figs. 6 and 8) and the second implantation of the two implantations is carried out after removal of the first mask (Figs. 12 and 13 are performed after the temporary gate electrode 54 is removed in Fig. 11), using a second mask (dielectric layer 90, Fig. 9) of which the edge coincides with the edge of the first mask (the temporary gate electrode 54 and the dielectric layer 90 overlaps as shown in Fig. 9) [claims 2 and 13];

characterized in that the first mask and the second mask are formed in a self-aligned manner (Figs. 5 and 10) [claims 3 and 14];

characterized in that the first mask is formed by a dummy gate region (temporary gate electrode 54 is used and then later removed as shown in Figs. 5-11) of a first dielectric material (temporary gate oxide 52, Figs. 10), and the first implantation is used to form the extensions of the source and drain regions (Figs. 6 and 8 together formed the first implantation in the source/drain extensions 60 and regions 80) [claims 4 and 15];

characterized in that for the amorphizing implantation ions are chosen from a group comprising Ge, Si, Ar or Xe (col. 3, lines 44-50) [claim 9];

characterized in that a part of the function of the amorphizing implantation is provided by one of the two opposite conductivity type implantations (buried amorphous region 120 is provided by Fig. 12 of the second implantation) [claim 10];

a semiconductor device comprising a field effect transistor obtained with a method as claimed in claim 1 (col. 1, lines 6-11) [claim 11].

10. As to claims 5 and 16, An discloses substantial features the claim invention (see paragraphs above) and further discloses:

characterized in that after the first implantation (Figs. 9-17) a uniform masking layer of a second dielectric material different from the first dielectric material is deposited on the semiconductor body (dielectric layer 90, Fig. 9) and is subsequently removed from the top of the dummy gate region (Figs. 9-10; col. 3, lines 35-36) which is then removed by selective etching (col. 3, lines 37-38 and col. 4, lines 28-32), the remainder of the masking layer forming the second mask for the second implantation (dielectric layers 90, Figs. 12-13) which is used to dope the neighboring part of the channel region (retrograde impurity region 130, Fig. 13).

However, An fails to disclose the subsequent removal of the uniform masking layer from the top of dummy gate region being chemical mechanical polishing.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by An, based on the information provided by An.

An discloses:

planarizing the surface of a conductive layer using chemical mechanical polishing (col. 4, lines 20-26).

Given the teaching of An, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying the method disclosed by An by employing the well known and conventional feature of chemical mechanical polishing, in order to planarize the dummy gate region using chemical mechanical polishing.

11. As to claims 6 and 17, An also discloses:

after the second implantation, a uniform gate region layer is formed on top of the semiconductor body (conductive layer 160, Fig. 16; Fig 16 is performed after Figs. 12-13) and is subsequently removed by chemical mechanical polishing from the top of the second mask which is then removed by selective etching (col. 4, lines 20-32).

12. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over An in view of Wu as applied to claim 1, and further in view of Lai et al. (US PGPUB 2002/0102801 A1 and Lai hereinafter).

13. As to claims 8 and 19, although An discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

characterized in that the source and drain regions are formed before the source and drain extensions.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by An in view of Wu, as evidenced by Lai.

Lai discloses:

characterized in that the source and drain regions are formed before the source and drain extensions (source/drain regions 108 are formed before the extension 114 is formed as shown in Figs. IC-1D).

Given the teaching of Lai, a person having ordinary skills in the art a the time of the invention would have readily recognized the desirability and advantages of modifying An in view of Wu by employing the well known or conventional feature of forming the source and drain regions before the source and drain extensions, such as disclosed by Lai, in order to avoid thermal process.

Response to Arguments

14. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAUN CAMPBELL whose telephone number is (571)270-3830. The examiner can normally be reached on Monday Through Friday 8:00AM-5:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Ha can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shaun Campbell/
Examiner, Art Unit 2829
9/16/2008

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829